Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A re-targetable communication processor, comprising:

a. a connectivity unit;

b. a digital signal processing core coupled to the connectivity unit;

c. a plurality of scaleable functional units, coupled to the connectivity unit, to execute mathematically intensive operations, further including:

a local memory;

a plurality of removable complex arithmetic elements (hereinafter CAE) coupled to one another~~, to the local memory~~ and to an inter-CAE bus, each of the plurality of CAEs to access the local memory and including a sequencer, a CAE memory, and an arithmetic unit, the sequencer to cause data to be sequenced from [[a]] the CAE memory to only the arithmetic unit and to cause only the arithmetic unit to execute an operation on the data; and

a bus controller coupled to the inter-CAE bus and the connectivity unit.

Claim 2 (currently amended): The re-targetable communication processor according to claim 1, the plurality of CAEs further comprising:

a. [[a]] the CAE memory to store data for the mathematically intensive operations;

b. a data router coupled to the CAE memory;

c. the arithmetic unit, coupled to the CAE memory and the data router, to execute operations in accordance with ~~the~~ control information; and

d. the data router to route data to the sequencer and the CAE memory and to facilitate communications among the CAEs in the scaleable functional unit.

Claim 3 (original): The re-targetable communication processor according to claim 2, the CAE memory further comprising:

two banks of separately addressable data memories.

Claim 4 (original): The re-targetable communication processor according to claim 3, the arithmetic unit further comprising:

a. a register file to accept data from the data memories; and

b. a plurality of multiplier-accumulator engines, coupled to one another, to the register file and to the data memories, to operate on the mathematically intensive operations.

Claim 5 (original): The re-targetable communication processor according to claim 4, the multiplier-accumulator engine further comprising:

a. a pre-adder to generate a first sum by adding data from the register file and the data memory;

b. a multiplier to generate a multiplier output by multiplying data from the data memories or the first sum;

c. an accumulator to generate a second sum by adding the multiplier output or data from the data memories; and

d. a data packing block to configure the second sum into a pre-defined format.

Claim 6 (original): The re-targetable communication processor according to claim 5, the multiplier further including a programmable shifter.

Claim 7 (cancel)

Claim 8 (original): The re-targetable communication processor according to claim 1, further including a micro-controller core coupled to the connectivity unit.

Claim 9 (currently amended): The re-targetable communication processor according to claim 2, wherein a first delay introduced by the sequencer ~~matches~~ is to match a second delay introduced by the arithmetic unit.

Claim 10 (currently amended): A scaleable functional unit in a re-targetable communication processor, comprising:

a. a local memory;

b. a plurality of removable complex arithmetic elements (hereinafter CAE) coupled to one another~~, to the local memory~~ and to an inter-CAE bus, each of the plurality of CAEs to access the local memory and including a sequencer, a CAE memory, and an arithmetic unit, the sequencer to cause data to be sequenced from [[a]] the CAE memory to only the arithmetic unit and to cause only the arithmetic unit to execute an operation on the data; and

c. a bus controller coupled to the inter-CAE bus and the connectivity unit.

Claim 11 (currently amended): The scaleable functional unit according to claim 10, the CAE further comprising:

a. [[a]] the CAE memory to store data for the mathematically intensive operations;

b. a data router coupled to the CAE memory;

c. the arithmetic unit, coupled to the CAE memory and the data router, to execute operations in accordance with ~~the~~ control information; and

d. the data router to route data to the sequencer and the CAE memory and to facilitate communications among the CAEs in the scaleable functional unit.

Claim 12 (original): The scaleable functional unit according to claim 11, the CAE memory further comprising:

two banks of separately addressable data memories.

Claim 13 (original): The scaleable functional unit according to claim 12, the arithmetic unit further comprising:

a. a register file to accept data from the data memories; and

b. a plurality of multiplier-accumulator engines, coupled to one another, to the register file and to the data memories, to operate on the mathematically intensive operations.

Claim 14 (original): The scaleable functional unit according to claim 13, the multiplier-accumulator engine further comprising:

a. a pre-adder to generate a first sum by adding data from the register file and the data memory;

b. a multiplier to generate a multiplier output by multiplying data from the data memories or the first sum;

c. an accumulator to generate a second sum by adding the multiplier output or data from the data memories; and

d. a data packing block to configure the second sum into a pre-defined format.

Claim 15 (original): The scaleable functional unit according to claim 14, the multiplier further including a programmable shifter.

Claim 16 (currently amended): The scaleable functional unit according to claim 10, the CAEs are coupled to one another via an east port, a west port and the inter-CAE ~~port~~ bus.

Claim 17 (currently amended): The scaleable functional unit according to claim 11, wherein a first delay introduced by the sequencer ~~matches~~ is to match a second delay introduced by the arithmetic unit.

Claim 18 (currently amended): A computer system, comprising:

a microprocessor coupled to a system bus;

a system controller coupled to the system bus; and

an input/output controller hub, coupled to the system controller and coupled to an input/output bus;

an add-in card, coupled to the input/output bus, further including:

a re-targetable communication system formed on a single integrated circuit, comprising:

a. a connectivity unit;

b. a digital signal processing core coupled to the connectivity unit;

c. a plurality of scaleable functional units, coupled to the connectivity unit, to execute mathematically intensive operations, further including:

i. a local memory;

ii. a plurality of removable complex arithmetic elements (hereinafter CAE) coupled to one another~~, to the local memory~~ and to an inter-CAE bus, each of the plurality of CAEs to access the local memory and including a sequencer, a CAE memory, and an arithmetic unit, the sequencer to cause data to be sequenced from [[a]] the CAE memory to only the arithmetic unit and to cause only the arithmetic unit to execute an operation on the data; and

iii. a bus controller coupled to the inter-CAE bus and the connectivity unit;

d. a media access control processor coupled to the connectivity unit.

Claim 19 (currently amended): The computer system according to claim 18, the CAE further comprising:

a. [[a]] the CAE memory to store data for the mathematically intensive operations;

b. a data router coupled to the CAE memory;

c. the arithmetic unit, coupled to the CAE memory and the data router, to execute operations in accordance ~~to the~~ with control information; and

d. the data router to route data to the sequencer and the CAE memory and to facilitate communications among the CAEs in the scaleable functional unit.

Claim 20 (original): The computer system according to claim 19, the CAE memory further comprising:

two banks of separately addressable data memories.

Claim 21 (original): The computer system according to claim 20, the arithmetic unit further comprising:

a. a register file to accept data from the data memories; and

b. a plurality of multiplier-accumulator engines, coupled to one another, to the register file and to the data memories, to operate on the mathematically intensive operations.

Claim 22 (original): The computer system according to claim 21, the multiplier-accumulator engine further comprising:

a. a pre-adder to generate a first sum by adding data from the register file and the data memory;

b. a multiplier to generate a multiplier output by multiplying data from the data memories or the first sum;

c. an accumulator to generate a second sum by adding the multiplier output and data from the data memories; and

d. a data packing block to configure the second sum into a pre-defined format.

Claim 23 (original): The computer system according to claim 22, the multiplier further including a programmable shifter.

Claim 24 (currently amended): The computer system according to claim 18, the CAEs are coupled to one another via an east port, a west port and the inter-CAE ~~port~~ bus.

Claim 25 (original): The computer system according to claim 18, wherein the re-targetable communication system further including a micro-controller core that is coupled to the connectivity unit.

Claim 26 (currently amended): The computer system according to claim 19, wherein a first delay introduced by the sequencer ~~matches~~ is to match a second delay introduced by the arithmetic unit.

Claim 27 (new): The re-targetable communication processor according to claim 1, wherein the re-targetable communication processor is formed of a single integrated circuit.